The GeekPort™

The GeekPort™ is a new feature connector unique to the Be™ System. It provides Digital and Analog I/O and D.C. Power through a 37 pin connector at the back of the chassis. This port is aimed at experimenters and small entrepreneurs so that they may bring unique functions to the Be system. The GeekPort™ is located on the ISA bus and can be accessed by the CPU, a PCI Busmaster card or an ISA Busmaster card.

Features:

2 Bidirectional data ports.

Each 8 bit port may be independantly configured as input only, or output with readback. This allows the user to configure the GeekPort™ as 16 inputs, 8 inputs & 8 outputs, or 16 outputs. The data ports are protected against shorts to power or ground.

4 A/D Pins

Each of the 4 pins can be routed to a high quality 12 bit A/D convertor. An analog signal ground reference pin is provided. The data A/D pins are protected against shorts to power or ground.

4 D/A Pins

Each D/A pin is connected to an independant 8 Bit D/A convertor. An analog signal ground refrence pin is provided. The data D/A pins are protected against shorts to power or ground.

11 Power & Grounds

2 pins at +5v, and one pin each of +12V and -12V are provided. The power pins are protected by fuses on the motherboard. 7 ground pins are provided. The shell of the connector is connected to chassis Ground for shielding.

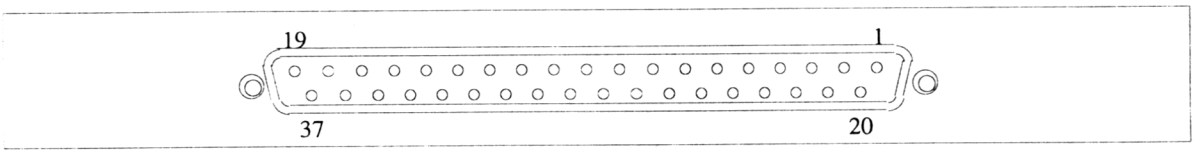

Fig.1 GeekPort™ Connector

Connector Description

The 37 Pin Female D-Shell connector was selected to best meet the requirements of experimenters

• High Pin Count

37 Pins allows for plenty of signal pins and adiquate power and grounds.

• Readily Available

The connector is listed in most electronics catalogs, and is available in most shops that cater to the experimenter.

• Mechanicaly Robust

The shell of the connector is rugged, and the pin spacing is large enough for inexperienced assemblers to solder connections to the pins. The large size of the connector will allow many types of devices to be built onto the connector itself or onto a small PCB dirctly connected to the connector, or within a standard backshell.

• Not standard on P.C.s

This connector is not comonly used on P.C.s so the risk of plugging an incompatable device into the connector is greatly reduced. Even if a user accidently attempts to connect a smaller connetor, the large size of the GeekPort™ connector prevents more than a few pins near the end from making contact.

The Power connections have specificaly been grouped to the center of the connector to help prevent the accidental shorting between the power pins of the GeekPort™ to external cables and devices.

GeekPort™ Technical Specifications

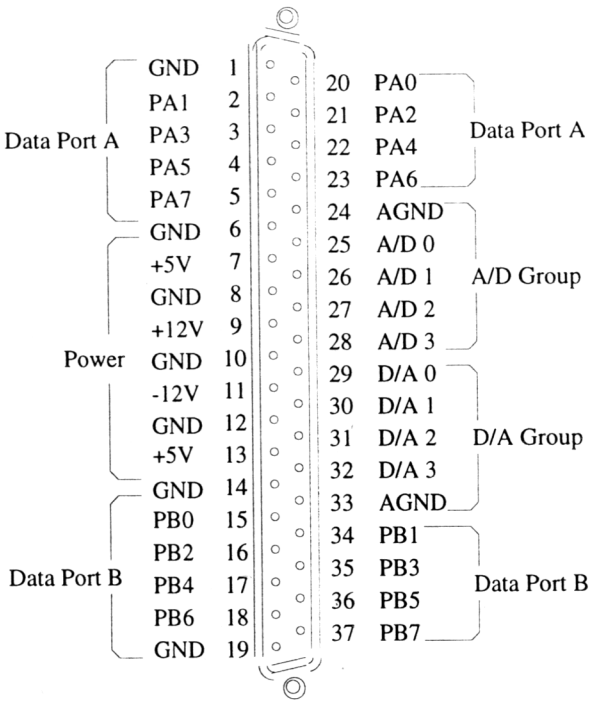

Fig. 2 GeekPort™ Pinout

Figure 2 shows the pinout of the GeekPort™ connector. The signals have been grouped into logical groups, with planning for direct circuit board connections of data ports. Note that the A/D and D/A groups each have an analog refrence ground (AGND) associated with them. This AGND should be used as the refrence for external op-amps or other analog circuitry, not as a power return path.

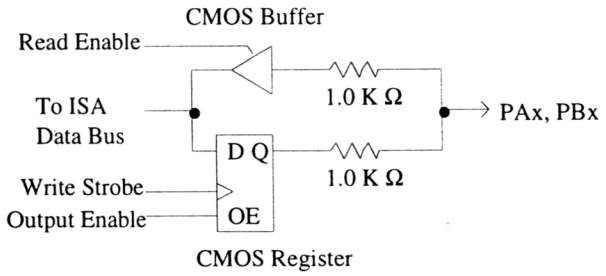

Fig 3. GeekPort™ Data Port Circuit

Figure 3 shows a typical bit of a data port. Note that the output of the CMOS buffer is isolated from the pin by a 1.0 KΩ resistor. The high value of this resistor restricts current flow to the output stage of the register in the case of short circuits or the accidental shorting of the connection to either +12V or -12V. If high drive capability is required, an external buffer should be added. Another 1.0 KΩ resistor is connected between the pin and the input to the data buffer. This resistor protects the input of the buffer, and by connecting to the pin through a second resistor, (rather than sharing one resistor) the input buffer can always read the actual state of the pin. This allows for the detection of short circuits to the

Data port pins, and it also allows an external device to force the state of a pin so that a port enabled as an output can also be used as an input.

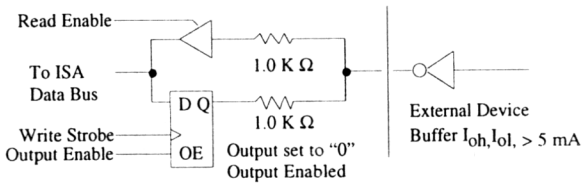

Fig 4. Overdriving a Data Output

Figure 4 shows the connection for using and output also as an input. The output drive capability of the register is 6 mA high or low. Since the output swing of the CMOS devices is from 0 to +5V, the 1K resistor will restrict the current flow to 5 mA, which is within the output drive specification. As long as the external device is capable of driving a 1 KΩ load, the voltage at the GeekPort™ pin will reflect the state of the external device, and reads to that Data port will read back the external forced value.
The 1.0KΩ resistor does add some minor delay (~50 nS) to the read path, but the inherent slow read cycle time of the ISA bus swamps this effect.

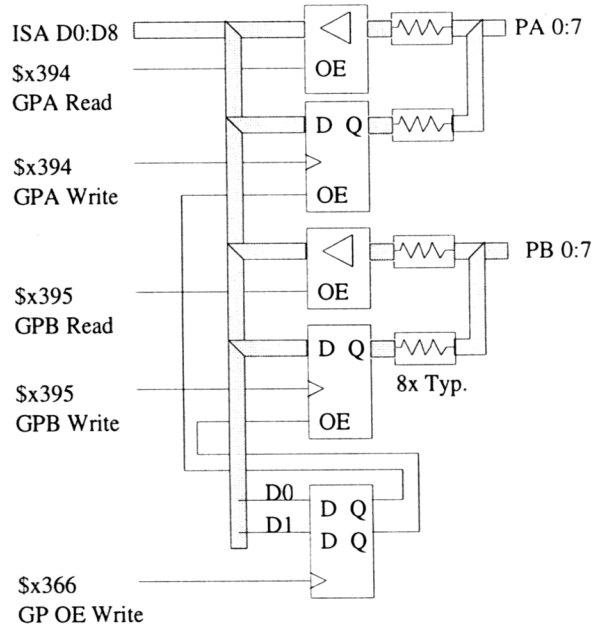

Fig. 5 GeekPort™ Data Path

Figure 5 is a logical representation of the GeekPort™ data path. Each port has a read and write address (Addresses shown are as seen from the 60x CPU) and a seperate register address that contains two bits that enable the outputs of the Data Port Registers. Upon reset the state of the Data Registers is unknown, and the outputs are disabled. Note that a read from a data port will return the value instantainously found at the data pins. It is the responsablity of the experimenter or developer to assure that either the voltage values are stable the time they are read, or that the data is re-sampled by software.

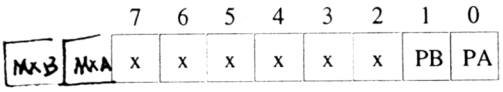

Fig. 6 GeekPort™ Output Enable Register

The output enables of the GeekPort™ are controlled through Bits 0 and 1 of the GeekPort™ Output Enable Register.

From	Type	Address
CPU	Memory	8000 0366
PCI	I/O	0000 0366
ISA	I/O Port	XXXX X366

word. swap it too r/o ???

Access: Read / Write
Must be accessed as a byte.

Bit	Description
0	High Enables the output of Data Port A Low Tristates the outputs of Data Port A
1	High Enables the output of Data Port B Low Tristates the outputs of Data Port B
2-7	Unused

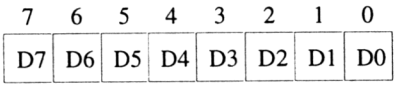

Fig. 7 GeekPort™ Data Port (A & B Typical)

Data Port A

From	Type	Address
CPU	Memory	8000 0394
PCI	I/O	0000 0394
ISA	I/O Port	XXXX X394

Data Port B

From	Type	Address
CPU	Memory	8000 0395
PCI	I/O	0000 0395
ISA	I/O Port	XXXX X395

Access: Read / Write

Bit	Description
0-7	Read: Reflects voltage of pin, 0 = Low 1 = High Write: Loads Digital Output Register with value. Data ports are accessed as bytes. A word reference to X394 will be converted to two seperate byte accesses.

NOTE: PB6 and PB7 are milti use bits,
PB6 is also an input Strobe that may be used used to start conversions of the A/D convertor. This pin is sampled by and 8 MHZ clock, conversions will start after the detection of a low to high transition on this pin. To guarentee detection the pin should be held high for at least 250nS
PB7 is also connected to the interupt controller, and may be used to directly intterupt the computer.

GeekPort™ Analog to Digital Conversion

The GeekPort™ uses an integrated 12 Bit A/D convertor to convert analog voltage levels to digital values. The A/D convertor has an 8 input multiplexer, inputs 0 - 3 are connected through current limiting resistors to input pins on the GeekPort™ connector, the other four inputs are used in the Joystick Circuity. The analog ground reference is also connected directly to a pin on the connector. For highest accuracy, the ground reference pin should be used as an analog voltage refrence only, no power return current should be directed through this pin.

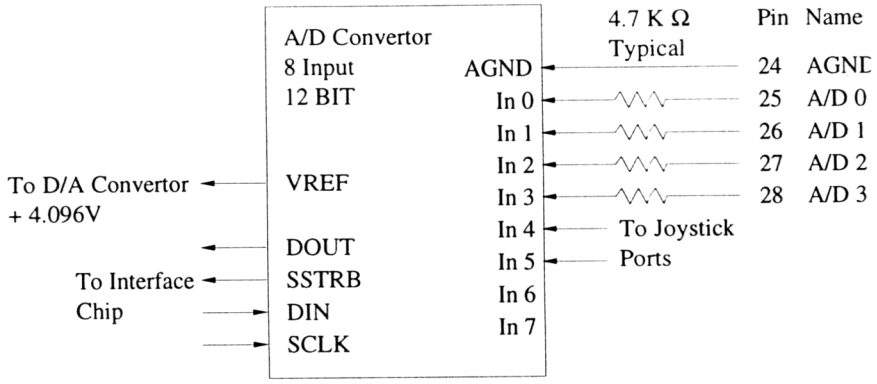

Fig. 8 GeekPort™ A/D Convertor Circuit

The analog input range is from 0 to 4.096 V, or -2.048 V to 2.048V. Control of the voltage range can be programmed for each conversion cycle. The A/D also supports differential voltage mesurements between A/D 0 and 1 or A/D 2 and 3. The 4.096V voltage range is based on the high accuracy voltage refrence (VRef) integrated into the A/D convertor, and coincidently produces a 1000 steps / Volt. External circuitry may be introduced to adjust the input voltage range and offset. The availability of ±12 volts on the GeekPort™ connector simplifies the addition of opamps to condition and scale input signals. The analog inputs are protected against short circuit to the ± 12V power pins.

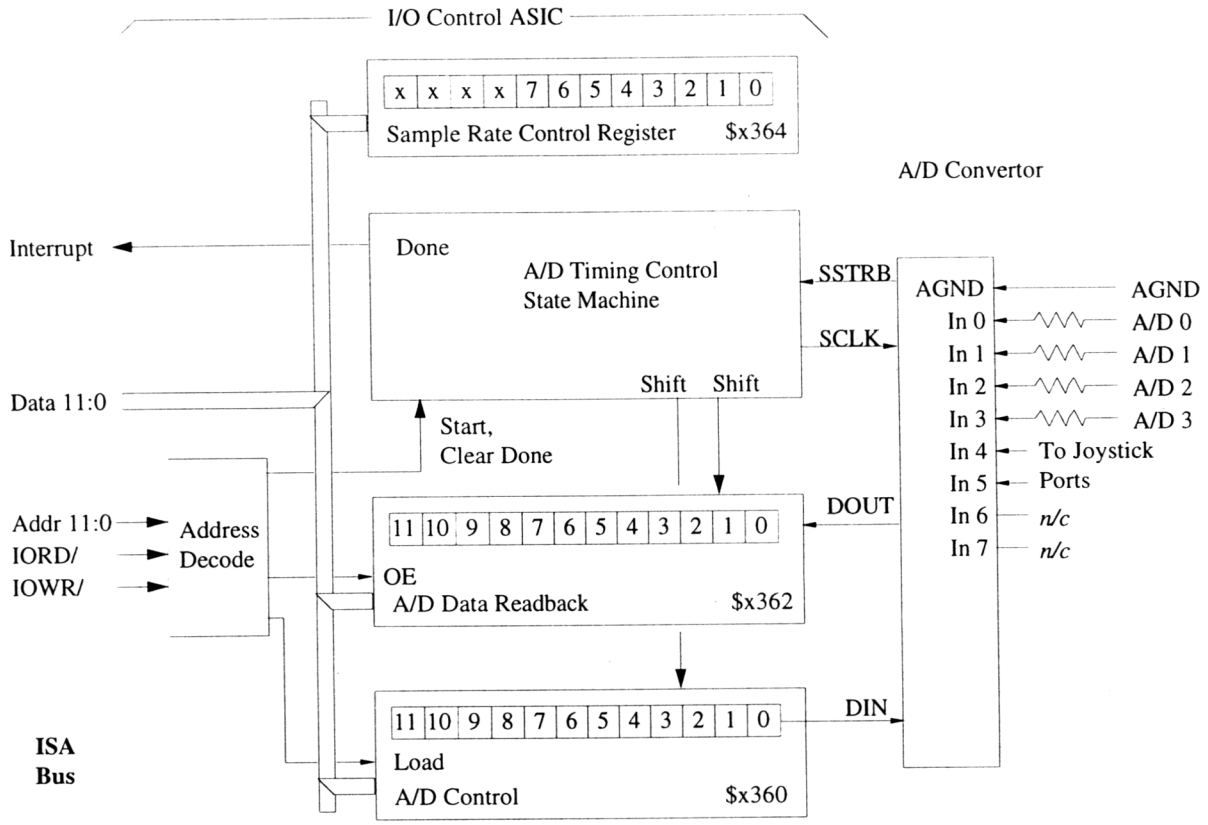

Fig.9 A/D Convertor Serial Interface

Access to the A/D convertor is through 3 registers, a 12 bit A/D control register , a 12 bit data read back register and an 8 bit programable sample rate register. An interrupt is generated at the completion of each conversion, and is cleared by a read of the data register. The control register may be read at any time to poll the state of the conversion. The Completion interupt is always enabled and is normaly masked in the interrupt controllers.

Three acquisition modes are supported: Single Shot; GeekStrobe sampling; and Programmed Sample Rate.

In **Single Shot** mode, one sample is taken each time the Control Register is written.

GeekStrobe mode allows hardware connected to the GeekPort to control the sample rate. Data bit 7 of GeekPort A becomes a strobe input to the sampling hardware; a sample is taken each time this input is pulsed. The maximum sample rate using GeekStrobe mode is 76kHz with no minimum. Base should be programmed to be 1.04167MHz when using GeekStrobe mode (see control register).

Programmed Sample Rate mode takes samples at regular time intervals; 512 sample rates are supported. Sample rates are calculated by the following equation:

sample rate = Base / (15 + (255 - M))

where:
Base can be programmed to be either 1.04167MHz or 1.38889MHz in the Control Register,
M is an 8 bit number programmed into the Sample Rate Control Register
its range is from 0 to 255.

For example, the highest sample rate possible would be:

Base = 1.38889 and M = 255,
Sample Rate = 1.3889MHz /15 = 92.593kHz

The lowest sample rate possible would be:

Base = 1.04167MHz and M = 0,
Sample Rate = 1.04167MHz /(15 + 255) = 3.858kHz

When a sample is captured in the data register using any of the three modes described above, the interrupt bit in the control register is set. This bit is brought out on a pin and is used to generate an interrupt to either or both PPC microprocessors, or the SW driver can poll the bit by reading the control register. The interrupt bit is cleared by a read of the A-D data register. No provision for the detection of missing the read of a sample in this mode has been made.

The conversion process is started by writing a byte to the control register. This byte specifies the input to be sampled, the input voltage range (0 to +Vref, or ± 1/2 Vref) and selects single ended or differential input. Other bits within the byte set the power saving and clock modes of the part. The I/O Control ASIC then sends the command byte to the A/D convertor. The A/D convertor aquires the analog voltage during the shifting of the command byte, then begins the conversion process. The I/O Control ASIC waits for the conversion process to complete (~10 µS) and shifts the result to the data register. The shifting of the last bit of the result into the data register sets a completion flag in the status register and can issue an interrupt to the main processor.

11	10	9	8	7	6	5	4	3	2	1	0
INT	MODE 1	MODE 0	BASE CLK	"0"	SEL2	SEL1	SEL0	UNI/ BIP	SGL/ DIFF	X	X

Fig 10. A/D Serial Control Register

A/D Serial Control Register

From	Type	Address
CPU	Memory	8000 0360
PCI	I/O	8000 0360
ISA	I/O Port	XXXX X360

Access: 16 bit Read / Write

Bit	Name	Description
0 - 1	X	Selects Clock and power down modes. Hard wired in asic The read state of these bits are not guarenteed. These bits are ignored on writes
2	SGL/-DIFF	1 = Single ended Mode 0 = Differential Input Mode
3	UNI/-BIP	1 = Unipolar - Voltage Range from 0 to 4.096V 0 = Bipolar Voltage reange from -2.048v to +2.048v
6 - 4	SEL 2 - 0	Select Inputs (Note: In single ended mode the input is not binary coded.) Single ended mode uses AGND as the differenceing input.

SEL

210	Single Ended Input Mode:
000 = CH0	A/D 0 Pin 25
100 = CH1	A/D 1 Pin 26
001 = CH2	A/D 2 Pin 27
101 = CH3	A/D 3 Pin 28
010 = CH4	Joystick A -From Multiplexer
110 = CH5	Joystick B -From Multiplexer
011 = CH6	Unused
111 = CH7	Unused

to read channel 6:

0,011,11,00 = 3C

7:

0,111,11,00 = 7C

SEL

210	Differential Input Mode:
000 = CH0	+ input A/D 0 Pin 25
CH1	- input A/D 1 Pin 26
001 = CH2	+ input A/D 2 Pin 27
CH3	- input A/D 3 Pin 28
010 =	Do not use - Joystick Port
011 =	Do not use - Joystick Port
100 = CH0	- input A/D 0 Pin 25
CH1	+ input A/D 1 Pin 26
101 = CH2	- input A/D 2 Pin 27
CH3	+ input A/D 3 Pin 28
110 =	Do not use - Joystick Port
111 =	Do not use - Joystick Port

7	Reserved	Reserved for future use. Returns 0 for reads. Write 0
8	Base Clock	Selects one of two frequencies to use to divide to create the sample rate 0 = 1.04167 MHz 1 = 1.38889 MHz These frequencies were chosen to create a fine and coarse range of clocks to produce equal spaced samples. Sample rates slower than can be achived by the programmable sample rate must be implemented single samples in software, or by external hardware triggering the Geekstrobe sample mode.
10-9	Mode	Sample Mode select 00 = Single sample mode. Each write to the Control register will cause a single conversion to take place. 01 = Geekstrobe sample. Samples will be taken and converted for each pulse of Bit 6 of the data port B 10 = Programmed Sample rate. The sample rate register must be set to the desired count before this mode is selected.
11	Interrupt	1 = Interrupt asserted, Conversion available to be read 0 = Interrupt not asserted, no valid data pending.

NOTE: This ia a 16 Bit register in ISA space. Due to endian issues the bytes within a word must be swapped prior to a write to the control register, and data returned must be swapped back.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	11	10	9	8	7	6	5	4	3	2	1	0

Fig 11. A/D Serial Data Register

A/D Serial Data Register

From	Type	Address
CPU	Memory	8000 0362
PCI	I/O	8000 0362
ISA	I/O Port	XXXX X362

Access: Read Only

Bit	Name	Description
11-0	Data 11-0	Contains data from A/D Cycle
15-12	Unused	Unused. Data will be undefined in these bits.

(It would have been far better to have the data aligned to D15 and have 3-0 report back "0", but to save pins on the I/O control chip, only 12 data bits have been implemented.)

NOTE: This ia a 16 Bit register in ISA space. Due to endian issues, the bytes within a word must be swapped after a read.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

FIG 12. Geekport Sample Rate Control Register

Geekport Sample Rate Control Register

From	Type	Address
CPU	Memory	8000 0364
PCI	I/O	8000 0364
ISA	I/O Port	XXXX X364

Access: Read/ Write
Byte or word access

Bit	Name	Description
7-0	M 7-0	Divider Index " M"

GeekPort™ Analog Output

The four analog outputs of the GeekPort™ are connected to a Quad monolithic 8-bit D/A convertor. The Voltage range of the D/ A convertor is from 0 to 4.080V, in 256 steps or 16 mV per step. Simple op amp circuits external to the Be system may be used to set the scale or add an offset to this voltage range.

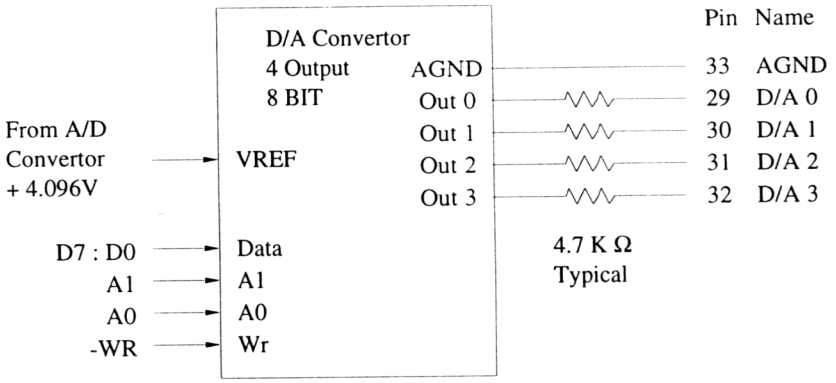

Fig 12 D/A Convertor Circuit

The 4 D/A convertors are active at the same time, and the output voltages are independantly adjustable. The D/A convertor appears as 4 I/O port addresses in the ISA space.

Note that each output is protected by a 4.7KΩ resistor, but no series resistor exists for the Analog Ground connection.

For best performace, external op-amp circuits should match the impedance of the voltage source with a matching 4.7KΩ impedance to AGND to prevent input offset currents.

<-------- Analog Design Voodo here, but it should be covered in the applications note for the GeekPort™.-------->

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Fig.13 GeekPort™ D/A Convertor register

D/A 0

CPU	Memory	8000 0390
PCI	I/O	8000 0390
ISA	I/O Port	XXXX X390

D/A 1

From	Type	Address
CPU	Memory	8000 0391
PCI	I/O	8000 0391
ISA	I/O Port	XXXX X391

D/A 2

From	Type	Address
CPU	Memory	8000 0392
PCI	I/O	8000 0392
ISA	I/O Port	XXXX X392

D/A 3

From	Type	Address
CPU	Memory	8000 0393
PCI	I/O	8000 0393
ISA	I/O Port	XXXX X393

Access: Write only

Bit	Description
0-7	Write: Loads Digital /Analog Convertor with Value to be converted. Note that the full Vref level is not achived with a data input of "FF". 1 LSB step = (VREF)*(2^-8) = 4.096 (1/256) = .016V 00 = 0V output 80 = 2.048V = 4.096V * (128/256) FF = 4.096V * (255/256)