GeekPort A-D Converter

Initial Version 0

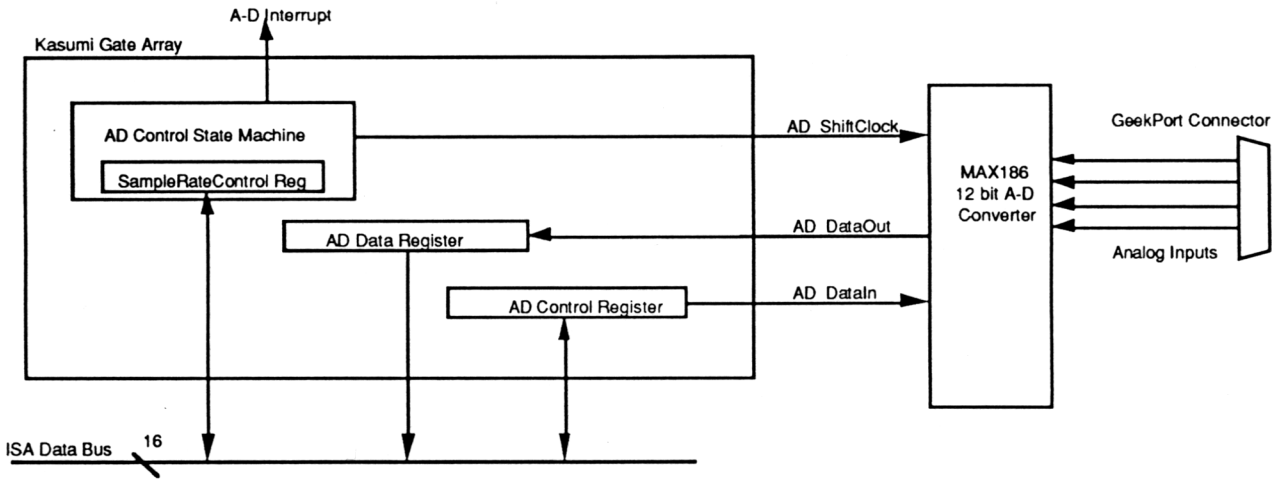
L. Thompson 12/13/94

Be, Inc. Confidential

General Description

One of the Be Computer's GeekPort features is a general purpose 12 bit A-D converter that can be used for data acquisition.

The GeekPort connector has four analog inputs that can be multiplexed and sampled by the A-D converter. The Kasumi gate array provides an interface and control function between the Be Computer's ISA bus and the Maxim MAX186 A-D converter chip. This is shown in the simplified block diagram below:



The MAX186 is a serial I/O 12 bit A-D converter chip. It requires its control register to be written each time a sample is taken, and samples are output in a serial stream with specific timing requirements for writing its register and reading data.

Kasumi provides a programmable interface and low-level state machine for programming and controlling the MAX186, making the interface for the software driver simple and efficient. The interface consists of three registers: the A-D control register provides a readback bit for the A-D interrupt, selects the acquisition mode, selects the base clock for the sample rate, and it holds five bits that are shifted out to the MAX186's control register for each sample; the A-D data register gathers the serial sample stream from the MAX186 and provides a parallel readback address for software; the Sample Rate Control (SRC) register holds an eight bit value that is used to divide down the sample rate in the Programmed Sample Rate mode.

Acquisition Modes

Three acquisition modes are supported: Single Shot; GeekStrobe sampling; and Programmed Sample Rate. In Single Shot mode, one sample is taken each time the Control Register is written.

GeekStrobe mode allows hardware connected to the GeekPort to control the sample rate. Data bit 7 of GeekPort A becomes a strobe input to the sampling hardware; a sample is taken each time this input is pulsed. The maximum sample rate using GeekStrobe mode is 76kHz with no minimum. Base should be programmed to be 1.04167MHz when using GeekStrobe mode (see control register).

Programmed Sample Rate mode takes samples at regular time intervals; 512 sample rates are supported. Sample rates are calculated by the following equation:

sample rate = Base / (15 + M)

where:
Base can be programmed to be either 1.04167MHz or 1.38889MHz
M is an 8 bit number programmed into the SRC register and can range from 0 to 255

For example, the highest sample rate possible would be:

Base = 1.38889 and M = 0,
Sample Rate = 1.3889MHz/15 = 92.593kHz

The lowest sample rate possible would be:

Base = 1.04167MHz and M = 255,
Sample Rate = 1.04167MHz/(15 + 255) = 3.858kHz

When a sample is captured in the data register using any of the three modes described above, the interrupt bit in the control register is set. This bit is brought out on a pin and is used to generate an interrupt to either or both PPC microprocessors, or the SW driver can poll the bit by reading the control register. The interrupt bit is cleared by a read of the A-D data register.

MAX186 Control Register

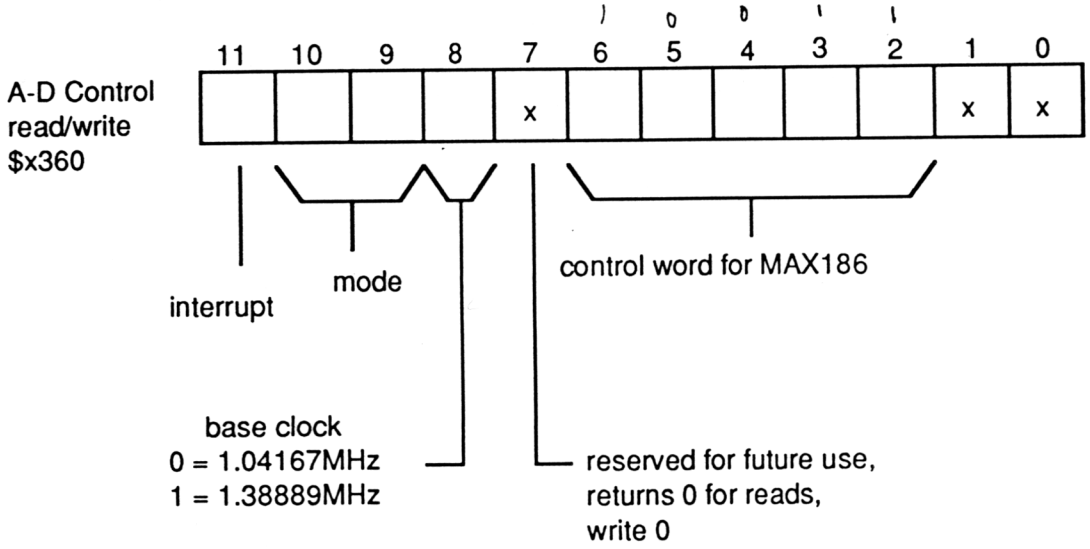
The MAX186 A-D converter chip has an 8 bit control register that must be programmed for each sample (see the data sheet for the MAX186). Kasumi simplifies this requirement for the SW driver by storing the contents to be programmed in the control register and shifting it into the MAX186 for each sample. Bit 7 is the start bit and is always a 1, and bits 1,0 select the clocking modes. In the Be implementation the external clocking mode is used exclusively. Since bit 7 is always a 1 and bits 1-0 are fixed, these bits are not programmable in the control register; Kasumi automatically shifts these bits into the MAX186. Bits 6 thru 2 are programmable in the control register.

Registers

Control Register, Address = $x360*

* Kasumi decodes only the lower 12 ISA addresses, ie AD 11:0

The Control Register is Read/Write, except bit 11 (the interrupt bit). Writes to this bit have no effect.



Interrupt: 1 = interrupt asserted
0 = interrupt not asserted

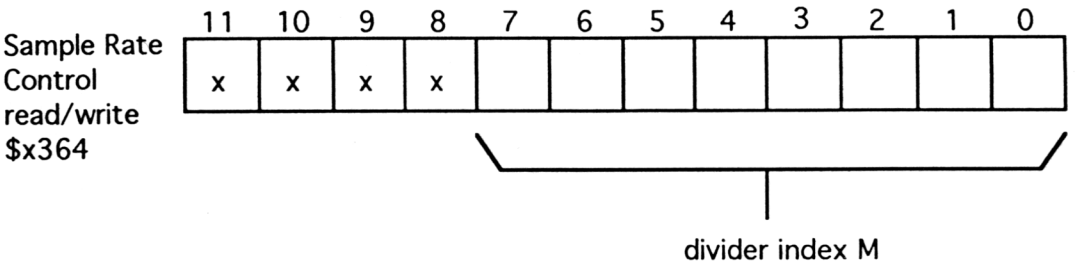
Note: Interrupt bit is set when a sample is available in Data register; interrupt bit is cleared when the data register is read.

Mode 00 = single sample
01 = GeekStrobe sample
10 = programmed sample rate
11 = reserved

Control Word:

bit 6 = A-D SEL2	(bit 6 in the MAX186)
bit 5 = A-D SEL1	(bit 5 in the MAX186)
bit 4 = A-D SEL0	(bit 4 in the MAX186)
bit 3 = UNI/_BIP	(bit 3 in the MAX186)
bit 2 = SGL/_DIF	(bit 2 in the MAX186)

Sample Rate Control Register; Address = $x364



Data Readback Register, read only; Address = $x362