Be System ISA Bus

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The Be system utilizes the 16 Bit ISA bus for most low bandwidth I/O devices. Wherever possible the standard ISA address space has been implemented, with the exeption of the features that are unique to the Be system and the location of two of the four Com ports, which have been moved to allow the ISA standard COM3 & 4 I/O addresses to be utilized by ISA Card modems (Which explect to be configured into a standard COM address)

The use of standard ISA addressing will permit the creation of a PCI based x86 card that could "Take over" the the motherboard and run shrink wrapped x86 opperating systems. In addition, future PowerPC chips may contain x86 interpreters, which could then directly run shrink wrapped x86 opperating systems.

The address Map of PReP describes a Non-Contiguous address mapping mode of the ISA address space. This permits 32 byte blocks of the I/O space to be mapped into 4k blocks of the main memory space, so that the ISA I/O space may be split into multible MMU entrys. Because the Be system will assign the same kernal MMU access attributes to each entry for the I/O space, no practicle use will be made of the Non-Contiguous address space. It may be desirable in the future to allow user level access to some I/O address blocks. The new Be specific I/O registers shall be grouped to maximize the number of unused protectable I/O address blocks. The I/O addresses map shall be clearly described in the user documentation to allow for easyer instalation of ISA Cards.

The GeekPort™ and Joystick implementations share hardware, so they must be controlled by the same driver, and cannot be split into individual protected address blocks. The GeekPort™, Joystick, Infrared interface, and LPT1 share an MMU Page.

Device	Component	Bus	I/O Address	Address Standard
5-16 bit ISA Slots	Connectors	ISA	x100-FFFF	(ISA)
Keyboard / Mouse	I8242	Y-Bus	x060, x064	(ISA)
Real Time Clock	BQ3285	Y-Bus	x070, x071	(ISA)
IDE ATA Interface	Buffers	Y-Bus	x1F0-x1F7, x3F6, x3F7	(ISA location)
SuperI/O Config	82091AA	Y-Bus	x398, x399	(PReP)
Parallel	82091AA	Y-Bus	x3BC- x3BE	(ISA PP1)
Floppy	82091AA	Y-Bus	x3F0- x3F7	(ISA Floppy)
COM1	82091AA	Y-Bus	x3F8- x3FF	(ISA Com 1)
COM2	82091AA	Y-Bus	x2F8- x2FF	(ISA Com 2)
GeekPort A/D CNTL	GeekPort	Y-Bus	x360- x361, 16 bit	(Be location)
GeekPort A/D DATA	GeekPort	Y-Bus	x362- x363, 16 bit	(Be location)
GeekPort A/D RATE	GeekPort	Y-Bus	x364, 8/16 bit	(Be location)
GeekPort OE	GeekPort	Y-Bus	x366	(Be location)
Joystick Address	Joystick	Y-Bus	x367	(Be location)
Infrared Interface (12Bit)	KASUMI	ISA	x368- x36A, 16 bit	(Be location)
COM3 (Be)	16C554	Y-Bus	x380- x387	(Be location)
COM4 (Be)	16C554	Y-Bus	x388- x38F	(Be location)
GeekPort D/A (8Bit)	GeekPort	ISA	x390- x393	(Be location)
GeekPort GPA	GeekPort	Y-Bus	x394	(Be location)
GeekPort GPB	GeekPort	Y-Bus	x394	(Be location)
Joystick Buttons	Joystick	Y-Bus	x397	(Be location)
MIDI 1 Port	16C554	Y-Bus	x3A0- x3A7	(Be location)
MIDI 2 Port	16C554	Y-Bus	x3A8- x3AF	(Be location)
Audio System	AD1848	Y-Bus	x830-x834	(PReP location)

Address Decodes:
The 12 bit I/O address space shall be decoded for each address.

Singal Name	Device	Function	Size	Decode Range	Additional Logic
-UART3	16C554	COM Port (3)	8	x380 - x387	--
-UART4	16C554	COM Port (4)	8	x388 - x38F	--
-MIDIACS	16C554	MIDI Port (1)	8	x3A0 - x3A7	--
-MIDIBCS	16C554	MIDI Port (2)	8	x3A8 - x3AF	--
-DAWR	DAC	GPDAC	4	x390 - x393	WR
-GPAWR	'574	GP Data port A	1	x394	WR
-GPARD	'245	GP Data port A	1	x394	RD
-GPBWR	'574	GP Data port B	1	x395	WR
-GPBRD	'245	GP Data port B	1	x395	RD
-JOYBTNOE	'245	Joystick Buttons	1	x397	RD
-CODECCS	Codec	Audio I/O	4	x830 - x833	--

Registered Outputs:
These are register bits in the I/O space implemented as logic within Kasumi. A "1" written to the I/O location will set the output pin, A 0 will reset it. Note that for the GPA bits, the output pin will be driven low if a "1" is writtn into that location

The 12 bit I/O address space shall be decoded for each address.

Singal Name	Device	Function	Size	Decode Range	Additional Logic
-GPAOE	Kasumi	GPA Output Enable	1	x366 Bit 0	Reg output, INVERT
-GPBOE	Kasumi	GPB Output Enable	1	x366 Bit 1	Reg output, INVERT
JOYMUX_A0	Kasumi	Joystick Mux Enable	1	x367 Bit 0	Reg output
JOYMUX_A1	Kasumi	Joystick Mux Enable	1	x367 Bit 1	Reg output

Buffer Control:
The Ybus contains all of the I/O devices listed above, and the Super I/O chip which contains the FDC, COM1 and COM2 the Parrallel port, And configuration Registers.

Singal Name	Device	Function	Size	Decode Range	Notes
-YBUSEO	'245	YBus Enable	32	x380 - x39F	(SuperI/O), GP,Joy,DA , COM3 & 4
			32	x3A0 - x3BF	MIDI 1 & 2, PP1 (Spare Bytes)
			16	x3F0 - x3FF	FLOPPY 1, COM1 (SuperI/O)
			8	x2F8 - x2FF	COM2 (SuperI/O)
			4	x830 - x833	Sound Codec
					IDE

GeekPort A/D registers:
Control of the serial A/D is through 3 registers within the ISA FPGA. A state machine is provided to control the timming of the convertor. A write to the ADCNTL register begins the conversion process. When the conversion is complete, the data is shifted into the ADDATA Data register and an interrupt is generated.

Register	Size	Address	Access
ADCNTL	12	x360	Read / Write
ADDATA	12	x360	Read Only, A Read Clears the Interrupt
ADCNT	8	x362	Read / Write

Infrared Interface:
Communications with the Infrared Microcontroller are through two registers, a transmit message register (IRTX) and a receive message register (IRRX).

Register	Size	Address	Access
IRTX	10	0368	Write Only
IRRX	11	036A	Read Only, A Read Clears Interrupt

ISA I/O Address Map

00-07		08-0F		10-17		18-1F	
000	DMA	008	DMA	010	DMA	018	DMA
020	INT CNTL & MASK	028		030		038	
040	TIMER PIT#1	048	TIMER PIT#2	050		058	
060	Keyboard & Mouse	068		070	RTC	078	
080	DMA Page & Channel	088		090	Port 92	098	
0A0	INT2	0A8		0B0		0B8	
0C0	DMA2	0C8	DMA	0D0	DMA	0D8	DMA
0E0	Coprocessor	0E8		0F0	COPROCESSOR	0F8	

00-07		08-0F		10-17		18-1F	
100		108		110		118	
120		128		130		138	
140		148		150		158	
160		168		170		178	
180		188		190		198	
1A0		1A8		1B0		1B8	
1C0		1C8		1D0		1D8	
1E0	IDE/ATA	1E8		1F0		1F8	

00-07		08-0F		10-17		18-1F	
200	ISA Game	208	ISA Game	210		218	
220		228		230		238	
240		248		250		258	
260		268		270		278	PP3
280		288		290		298	
2A0		2A8		2B0		2B8	
2C0		2C8		2D0		2D8	
2E0		2E8	COM4	2F0		2F8	COM2

00-07		08-0F		10-17		18-1F	
300		308		310		318	
320		328		330		338	
340		348		350		358	
360	A/D CNTL Low	368	IR	370	Floppy 2	378	PP2
361	A/D CNTL High	369	IR	371	Floppy 2	379	PP2
362	A/D DATA Low	36A	IR	372	Floppy 2	37A	PP2
363	A/D DATA High	36B	IR	373	Floppy 2	37B	PP2
364	A/D CNT Low	36C	(Reserved)	374	Floppy 2	37C	PP2
365	A/D CNT high (res.)	36D	(Reserved)	375	Floppy 2	37D	PP2
366	GPA/B OE	36E	Joystick Address Mux	376	Floppy 2	37E	PP2
367	(Reserved)	36F	Joystick Address Mux	377	Floppy 2	37F	PP2
380	SERIAL 3	388	SERIAL 4	390	D/A 0	398	SIO ctl
381	SERIAL 3	389	SERIAL 4	391	D/A 1	399	SIO ctl
382	SERIAL 3	38A	SERIAL 4	392	D/A 2	39A	
383	SERIAL 3	38B	SERIAL 4	393	D/A 3	39B	
384	SERIAL 3	38C	SERIAL 4	394	GPA	39C	
385	SERIAL 3	38D	SERIAL 4	395	GPB	39D	
386	SERIAL 3	38E	SERIAL 4	396	(Reserved)	39E	
387	SERIAL 3	38F	SERIAL 4	397	JOYBUTTON	39F	
3A0	MIDI 1	3A8	MIDI 2	3B0	PP1	3B8	(Reserved)
3C0	VGA	3C8	VGA	3D0	VGA	3D8	VGA

3E0 PCMCIA 3E8 COM3 3F0 Floppy 1/ IDE/ATA 3F8 COM1

Interrupts:

Due to the high number of interrupt sources from built in resources on the Be system, It is impossible to use the standard 8259 controller pair (Part of the SIO) to field all of the interrupts and still leave room for PCI and ISA slot interrupts. A second Interrupt detection circuit made up of the Master and Slave FPGAs.

	Interrupt Source	Master/Slave		SIO
0	(Write Control Bit, Internal)	0	-	-
1	SMI_0 (Internal)	1	SMI_0	-
2	SMI_1 (Internal)	2	SMI_1	-
3	Not Used	3	N/C	-
4	ISA SLOT B24 / Serial 1	4	ISA SLOT IRQ4	IRQ4
5	ISA SLOT B25 / Serial 2	5	ISA SLOT IRQ3	IRQ3
6	Serial 3	6	Serial 3	-
7	Serial 4	7	Serial 4	-
8	MIDI 1	8	MIDI 1	-
9	MIDI 2	9	MIDI 2	-
10	SCSI	10	SCSI	(Muxed in SIO)
11	PCI SLOT 0	11	PCI SLOT 0	(Muxed in SIO)
12	PCI SLOT 1	12	PCI SLOT 1	(Muxed in SIO)
13	PCI SLOT 2	13	PCI SLOT 2	(Muxed in SIO)
14	SOUND SYSTEM	14	SOUND SYSTEM	-
15	Keyboard	15	Keyboard	IRQ1
16	RTC	16	ISA IRQ8	/IRQ8 / RTC
17	ISA SLOT B23	17	ISA IRQ5	IRQ5*
18	ISA SLOT B22 / FDC	18	ISA IRQ6	IRQ6
19	ISA SLOT B21 / LPT 1	19	ISA IRQ7	IRQ7
20	ISA SLOT B4	20	ISA IRQ9/2	IRQ9*
21	ISA SLOT D3	21	ISA IRQ10	IRQ10*
22	ISA SLOT D4	22	ISA IRQ11	IRQ11*
23	ISA SLOT D5 / Mouse	23	ISA IRQ12	IRQ12
24	ISA SLOT D7 / IDE	24	ISA IRQ14	IRQ14
25	ISA SLOT D6	25	ISA IRQ15	IRQ15*
26	From SIO ISA 8259*	26	From SIO ISA 8259*	-
27	IR µController	27	IR µController	-
28	GP A/D	28	GP A/D	-
29	GP Pin Interrupt	29	GP Pin Interrupt	-
	Not Used	-		IRQ13
	System Timer	(26)		IRQ0

* These interrupts are not used by the built in I/O devices. The SCSI and PCI interrupts may be multiplexed onto any of these interrupts if the use of the 8259 is desired.

The output of the system Timer is not available as an external pin on the SIO, Interrupts from the system timers must pass through the 8259 Interrupts controllers (Inside the SIO) .
The 8259 should be programmed to only pass these interrupts when in Be mode.

INTERRUPTS

IRO		System Timer	Standard	
IR1		Keyboard	Standard	
IR2		(Cascade)	Standard	
IR3	*	COM2	Standard	
IR4	*	COM1	Standard	
IR5	*			(Parallel Port 2)
IR6	*	FDC	Standard	
IR7	*	Parallel Port 1	Standard	
IR8		Real Time Clock	Standard	
IR9	*			(PCI SCSI on David's Board)
IR10	*	Sound System Interrupt	Be/Sound card Standard	
IR11	*			
IR12	*			PS 2 Mouse?
IR13		Numeric Coprocessor		
IR14	*	Hard Disk (IDE)		
IR15	*			

DMA Controller Allocations